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In situ SEM observation of electromigration phenomena in fully embedded copper interconnect structures

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Abstract

An experimental set-up is presented, that allows in situ scanning electron microscope (SEM) investigations of the progress of electromigration damage in fully embedded copper interconnect structures. A LEO Gemini 1550 SEM has been equipped with a heating stage and electrical connections for the experiment. The studied interconnect structures are usually used for reliability testing in electromigration ovens. These test structures are located within the scribelines of wafers. Therefore, they allow the characterization of the electromigration behaviour of products on the wafer. To enable the SEM observation, focused ion beam (FIB) was used to prepare cross-sections of the samples maintaining their electrical functionality. Thereby, a thin layer of passivation was left over in front of the interconnects to keep them fully embedded. The SEM images which were taken at an angle of 60° allow the observation of both the entire via/contact and the connecting lines. Multiple images were recorded during the degradation experiments. The resulting video sequences provide a good visualization of the formation, growth and motion of voids at the stressed interconnects. The dominant diffusion path has been identified.

Keywords: SEM; In situ; Electromigration; Dual–inlaid; Copper interconnect; Cross-section

1. Introduction

Electromigration and stress-induced degradation phenomena are reliability concerns for integrated circuits fabricated with inlaid copper technology. Highly integrated microprocessors require dense interconnects with dimensions down to some 100 nm. With the resulting increase in current density, the electromigration issue becomes more and more challenging. Additionally, several different interfaces are present around the inlaid copper interconnect structures providing diffusion paths for the copper atoms.

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The effective diffusion coefficient for the atomic transport in such an interconnect is described as the sum of contributions of several components [1]:

$$D_{\text{eff}} = D_{\text{b}} + D_{\text{gb}}\left(\frac{\delta_{\text{gb}}}{d}\right) + D_{\text{Cu/b}}\delta_{\text{Cu/b}}\left(\frac{2}{w} + \frac{1}{h}\right) + D_{\text{Cu/N}}\left(\frac{\delta_{\text{Cu/N}}}{h}\right) \quad (1)$$

with the diffusion coefficient D_{b} for the bulk material, D_{gb} for the grain boundary diffusion, $D_{\text{Cu/b}}$ for the diffusion along the copper/barrier interfaces and $D_{\text{Cu/N}}$ for the diffusion along the copper/caplayer interface. The diffusion coefficient D_{b} can be neglected for temperatures well below the melting point ($T < 0.5T_{\text{m}}$). The other three contributions to the effective diffusion coefficient are functions of the materials and materials combination (interface structure) and the interconnect geometry as well.

Hu et al. performed SEM studies at cross-sectioned post-mortem three-level copper dual–inlaid interconnects after electromigration tests. They explained the failures, which resulted from void growth in the line/via vicinity by interface-diffusion dominated mass transport along the Cu/SiN*x* interface [2].

In situ SEM investigation of unpassivated copper lines showed that electromigration induced degradation is caused by void formation mainly at the sidewall and next to blocking grains [3]. The fact that voids are formed at the sidewall and at the believed main diffusion path copper/caplayer interface underlines the importance of the investigation of fully embedded interconnect structures.

Therefore, in this study the samples under investigation were prepared to cross-sections using FIB, while maintaining their electrical functionality. Thereby, a thin layer of passivation was left over in front of the interconnect to keep them fully embedded. In situ SEM observations at an angle of 60° allow the assessment of degradation mechanisms at all visible interfaces and at the cross-section of the via.

2. Test structures for lifetime experiments

Suitable test structures are necessary in order to monitor the effect of process changes on reliability of microelectronic products. Such test structures usually reside within the scribline of a wafer. Therefore, they allow the characterization of the electromigration behaviour of products on the wafer. Sets of samples are tested under accelerated conditions and mean times to failure are determined. Activation energies E_{A} for the diffusion process are calculated using Black's law. An extrapolation provides an estimate for the lifetime of the product under real-life conditions.

The principle design of the electromigration test structure used in these experiments is shown in Fig. 1. The structure consists of an array of metal lines, the middle one is the line under test. Depending on which level of metallization is tested, this array of lines is either metal 1 or metal 2.

When metal 1 is tested, then the connecting wide metal lines (dashed lines) are in metal 2 level and the line under test is connected by one via at each end of the line. When metal 2 is tested, the connections to the bond pads are in metal 1 level. In this case, the vias at the ends of the line are part of the device under test.

The fact that the vias at the end of the line belong to the device under test for metal 2 is quite important for the electromigration degradation mechanism and for destructive failure analysis after lifetime experiments. Fig. 2 shows a schematic cross-section of the electromigration test structures

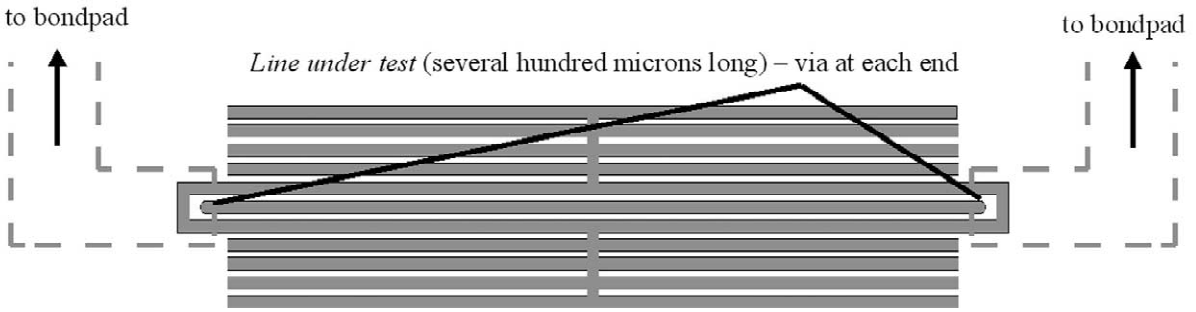

Fig. 1. Scheme of the electromigration test structure—for cross-section see Fig. 2.

used in the experiments with a two-level copper interconnect. The samples were fabricated in dual-inlaid copper technology, using PVD-tantalum for the barrier and PECVD-Si_3N_4 (PEN) as caplayer for the metal lines.

3. Post-mortem failures of samples after lifetime experiments

In order to understand the degradation mechanisms of interconnect structures, lifetime experiments are performed on a routine basis. Sets of samples are subjected to high current densities at elevated temperature. During oven experiments, the line resistance of the interconnect is monitored in order to terminate the test after a certain increase in electrical resitivity, usually about 10%, is reached.

Afterwards, the test structures are cross-sectioned using of FIB for failure analysis. Fig. 3 shows typical failure features at the cathode end of the line under test for such experiments. Although all three samples belong to the same wafer, the failure appearance found in post-mortem analysis is very different. In Fig. 3-1, the Cu/PEN interface seems to be the 'weakest interface', acting as the initial location for the material transport. In Fig. 3-2, a fatal void was formed inside the via, leaving behind flat surfaces, which are believed to be at the position of former grain boundaries. The via in Fig. 3-3 exhibits a combination of the two mechanisms described.

Keller et al. studied local textures and grain boundaries in voided unpassivated interconnect structures using electron backscattered diffraction (EBSD). They found, that the grains surrounding a void had a weaker Cu(111) texture than grains away from the voids [4].

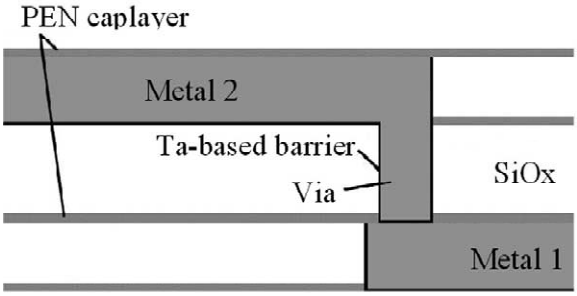

Fig. 2. Scheme of the cross-section of dual–inlaid copper interconnects.

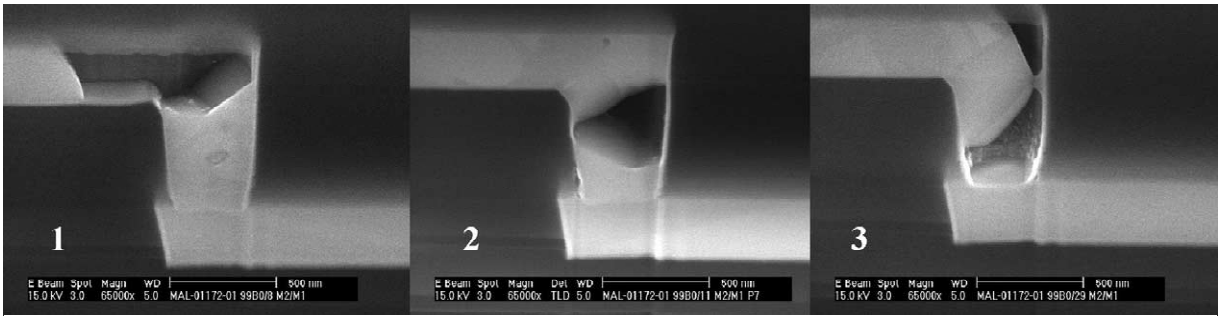

Fig. 3. Typical failure features after electromigration experiments.

In situ investigations of the void formation, growth and movement of such defects can provide time-resolved information about the degradation mechanisms and the dominant diffusion paths for material transport.

4. Experimental set-up for in situ investigation in a LEO Gemini 1550 SEM

The stage of a LEO Gemini 1550 SEM was replaced by a custom-made heating stage. This stage was manufactured by CVM Chemnitz (Germany). It consists of a aluminum base plate that can be mounted on the *xy*-stage of the SEM. A vertical glass rod, which holds the sample holder, is fixed to the base plate. An S-shaped THERMOCOAX wire heating element of 10-cm active length runs inside this holder. It is powered by a standard laboratory DC power supply. The power applied to it ranges from 5 to 10 W for temperatures up to 350 °C. This heater block can also be tilted manually tilted to approximately 50–70°, in order to view the samples, which contain FIB-milled cross-sections at the region of interest. A heat shield is mounted just below the sample holder.

Fig. 4 shows the heating stage inside the chamber. The glass rod and the heat shield are designed to

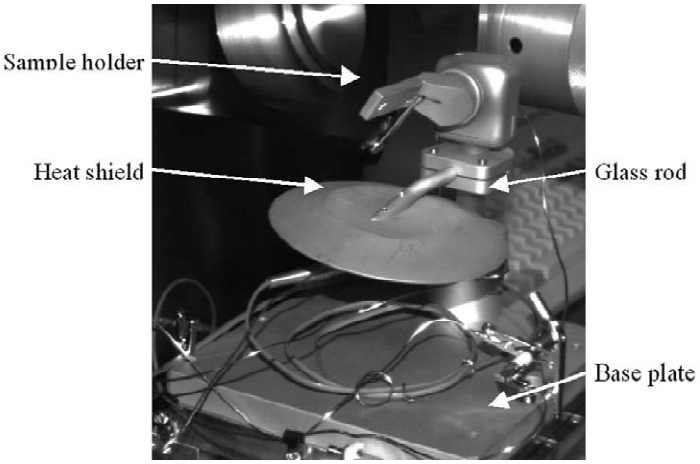

Fig. 4. SEM chamber with heating stage and wiring.

reduce the thermal load to the stage mechanism during the in situ experiment. A thermocouple is mounted near the sample to monitor the temperature during the experiments.

After the samples were mounted inside the SEM and the sample temperature had been stabilized, the electrical current was applied to the samples and the SEM image capturing started. The SEM imaging conditions were: 20 kV, 60-μm aperture, SE detector (Everhart-Thornley) at 400 V bias, 20-s frame capture time. Images were recorded automatically in 1–2-min intervals using a software macro.

5. Sample preparation

Samples were cleaved from the wafer scribeline and mounted on 24-pin test chips. The electrical connections were made by wire bonding from the aluminium bond pads to the landing pads of the test chip. Cross-sections were milled at the via site near the cathode end of the line under test using FIB for the in situ investigations. The following steps were performed sequentially:

1. the region of interest was locally coated with platinum;
2. a large trench was milled near the cathode end of the line under test'
3. using the fine milling tool, the final cross-section was milled, leaving a thin film of passivation in front of the via/line structure to keep it fully embedded;
4. depending on the test structure, connections to other test structures nearby were cut in order to avoid shorts.

The platinum deposition at the beginning of the procedure also helped to reduce charging effect during SEM imaging. However, the most crucial step in this preparation procedure is the final cross-section milling. The milling process was stopped just before the line under test was reached, leaving between 50 and 150 nm of passivation in front of the line and the via. With this procedure, the line and via under test was kept fully embedded.

Fig. 5 shows backscattered electron images of the final cross-section at two different acceleration voltages. The line under test cannot be seen at 5 kV, while it is visible at 15 kV. This proofs that there is still passivation in front of the line and the via.

6. Results and discussion

During the in situ the experiment, a sample with the line under test in metal 2 level was stressed at a temperature of 250 °C and at a current density of about 20 MA/cm^2. Fig. 6 shows a representative secondary electron image sequence. The experiment lasted for 35 h. The electron flux was from right to left in the images, and upwards through the via.

During the experiment, voids were seen first on top of the metal 2 trench (images 1–4). Initial shallow voids remained at their position until a certain (critical) size was reached. Eventually, they moved along the trench towards the end of the line. There, they merged into a larger void which subsequently started to grow from top to bottom into the via. Interestingly, the growth rate of this void was not constant. Additionally, the copper, which had been removed from the lower part of the via, was redeposited at the upper part of the via, since the horizontal extension of the void clearly

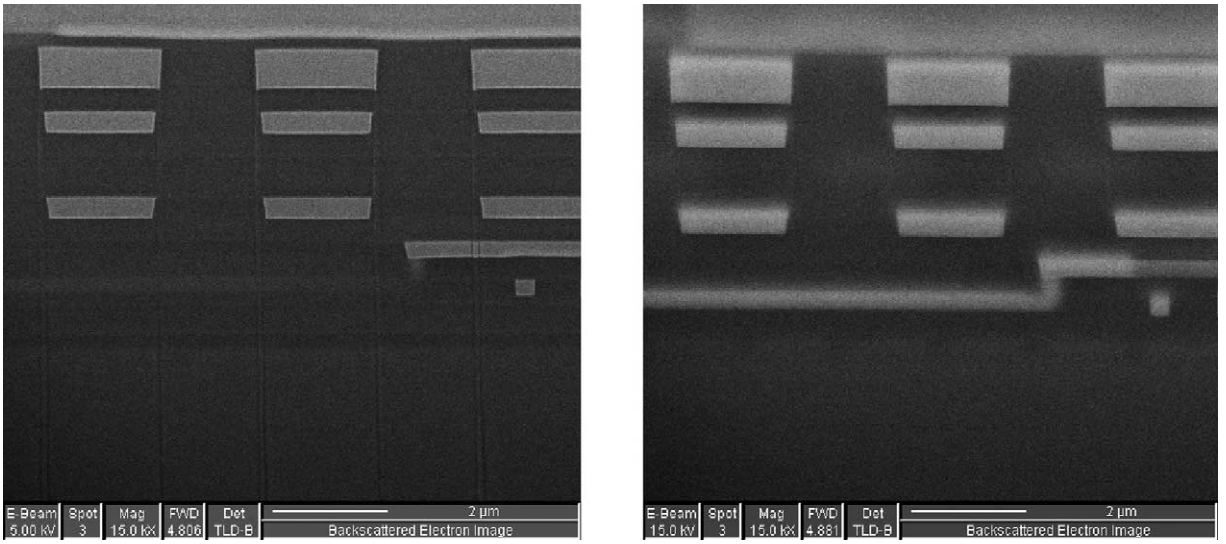

Fig. 5. Backscattered electron images at 5 kV (left) and 15 kV (right), illustrating the passivation in front of the line under test (in this case metal 1).

decreased in this region (images 13–16). The last image of the sequence shows the final state after 35 h. Although approximately 50% of the copper was removed from the via, a resistance increase of only 2% was measured.

After the in situ experiment had been terminated, the sample was FIB-cut perpendicular to the original cross-section in order to study the inner structure of the final void. The cross-section of the stressed via in Fig. 7 revealed that the shape of the final void is determined by the copper microstructure. The straight edges across the lower part of the via are believed to be located at the position of former grain boundaries. In the upper part, the redeposited material did not show grain boundaries, which leads to the conclusion that a single grain had been formed. The microstructure-dependent shape of the void explains its discontinuous growth rate, too. Once an inner surface has been formed, the void growth process seems to be dominated by surface diffusion. Depending on the crystallographic orientation of the grain next to the void, the diffusion rate will be different and, therefore, grains with different orientation will be disintegrated at different speeds.

The high directed material transport rate during the whole experiment confirms the expected high diffusion coefficient $D_{\mathrm{Cu/N}}$ for the diffusion along the copper/caplayer interface. However, this effect is exceeded once material transport into the upper part of the via and the subsequent redeposition starts.

Furthermore, the cross-section in Fig. 7 shows the remaining passivation in the original cross-section. The thickness of the passivation was between 80 and 110 nm. The original cross-section was covered with platinum in order to preserve the remaining passivation while preparing the second cross-section to the middle of the via. This proofs again that the line and the via under test were fully passivated during the in situ experiment.

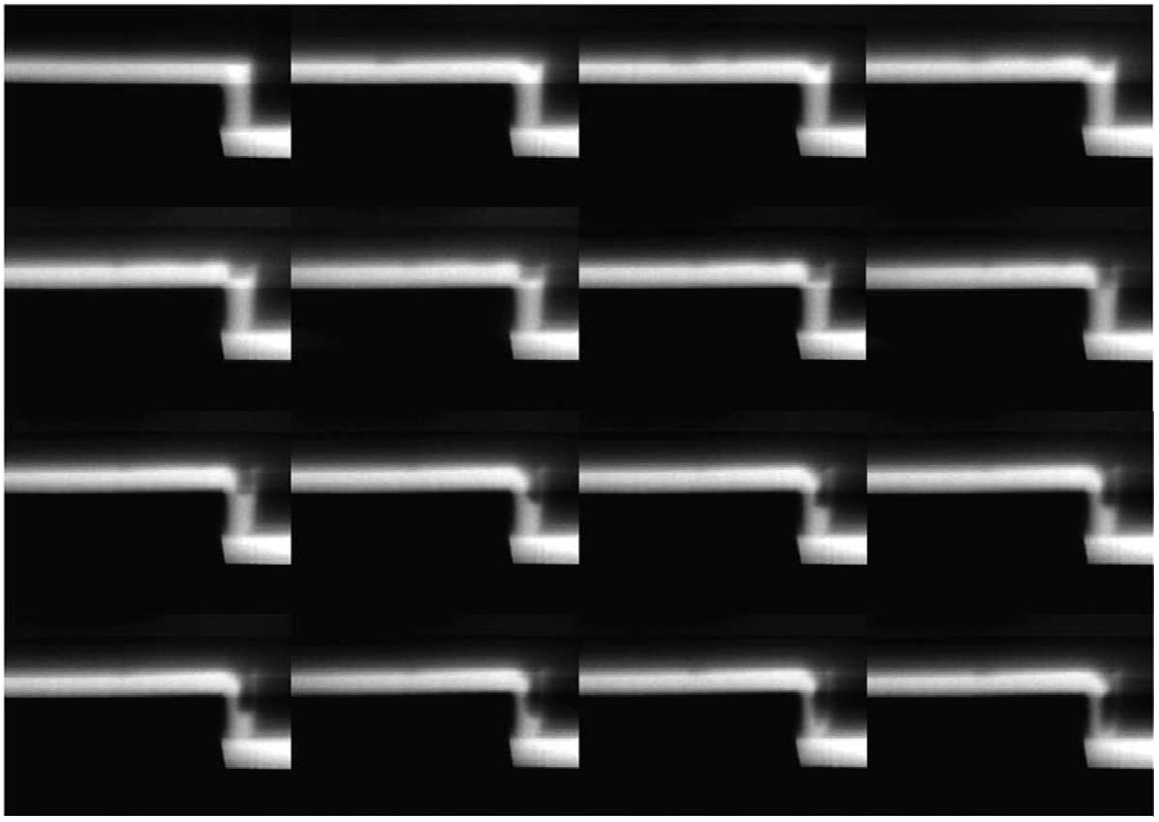

Fig. 6. Secondary electron image sequence that shows the development of voids at the cathode end of the test structure. (The time difference between two images is 2 h. For the video sequence, images were taken in 2-min intervals.)

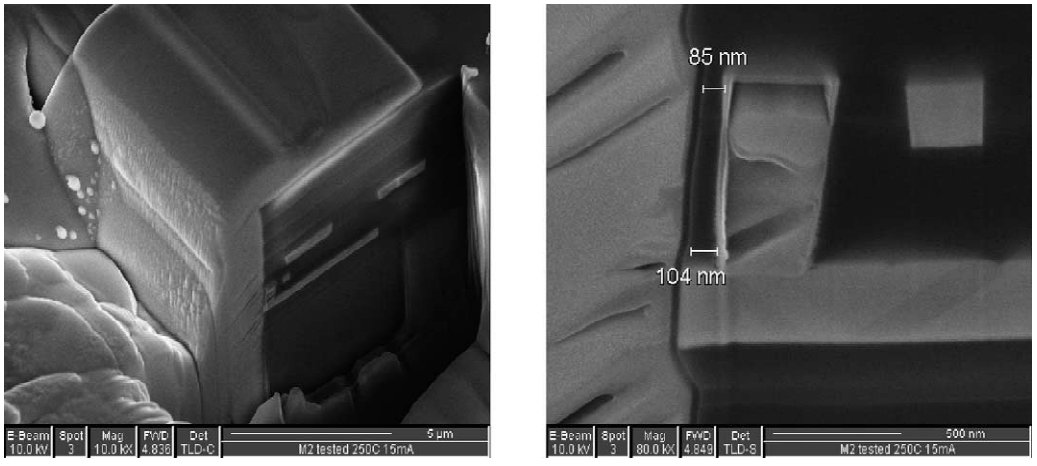

Fig. 7. FIB cross-section through the stressed via. Illustration of the preparation procedure (left), cross-section (right). The current direction is perpendicular to the image plane.

7. Conclusions

An experimental set-up has been demonstrated, which enables in situ studies of electromigration phenomena on fully passivated cross-sections of multilevel copper interconnects. The void formation process was visualized, and cross-section analysis after the in situ experiment revealed a relationship between the microstructure of the via and the non-constant growth rate of the void. Secondary electron imaging provided good resolution and contrast even for imaging through a passivation layer of about 100 nm.

This study gives evidence for theoretical models which postulate that voids grow at sites of flow divergences like grain-boundary triple points and interfaces [5]. Void formation, growth and movement, and consequently degradation, depend clearly on the grain structure of individual vias.

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